IN THE CLAIMS:

Please cancel claims 13. **Please also amend** claim 1 **and add** new claim 14-19, as shown in the complete list of claims that is presented below.

Claims 1 and 2 (cancelled).

3. (currently amended): A dry etching method for a semiconductor device, comprising the following steps of:

implanting a first region of a polysilicon layer with N type ions, the first region having a first area;

implanting a second region of the polysilicon layer with P type ions, the second region having a second area; and

simultaneously gate-etching an N type polysilicon gate electrode from the first region, a P type polysilicon gate electrode from the second region, and a non-doped polysilicon body from a non-doped region of the polysilicon layer during a two-stage etching ~~process; and~~ process, the N type polysilicon gate electrode occupying an area that is smaller than the first area, the P type polysilicon gate electrode occupying an area that is smaller than the second area, and the non-doped polysilicon body occupying an area that is ~~setting an etching area occupied by the non-doped polysilicon body, which is adjacent to at least one of the N type polysilicon gate electrode and the P type polysilicon gate electrode,~~ larger than a total area [[of]] occupied by the N type polysilicon gate electrode and the P type polysilicon gate electrode,

wherein an end point detection of one of the stages of the etching process is based on the etching of the non-doped ~~silicon~~ polysilicon body.

Claim 4 (cancelled).

5. (previously presented): The dry etching method according to claim 3, wherein the two-stage etching includes a first stage using a mixed gas of HBr and O_2 and a second stage using a mixed gas of HBr, O_2 and He.

Claims 6-10 (cancelled).

11. (previously presented): The dry etching method according to claim 3, wherein the N type polysilicon gate electrode and the P type polysilicon gate electrode are disposed adjacent one another.

Claims 12-13 (cancelled).

14. (new): The dry etching method of claim 3, wherein the non-doped polysilicon body is disposed adjacent to at least one of the N type polysilicon gate electrode and the P type polysilicon gate electrode.

15. (new): A dry etching method for a semiconductor device, comprising:

implanting a first region of a polysilicon layer with N type ions, the first region having a first area;

implanting a second region of the polysilicon layer with P type ions, the second region having a second area; and

simultaneously etching an N type polysilicon gate electrode from the first region, a P type polysilicon gate electrode from the second region, and a non-doped polysilicon body from a non-doped region of the polysilicon layer during an etching process, the N type polysilicon gate electrode occupying an area that is smaller than the first area, the P type polysilicon gate electrode occupying an area that is smaller than the second area, and the non-doped polysilicon body occupying an area that is smaller than a total area occupied by the N type polysilicon gate electrode and the P type polysilicon gate electrode,

wherein the etching process includes at least one etching stage in which end point detection is based on the etching of the non-doped polysilicon body.

16. (new) The dry etching method according to claim 15, wherein the non-doped polysilicon body is disposed adjacent at least one of the P type polysilicon gate electrode and the N type polysilicon gate electrode.

17. (new) The dry etching method according to claim 15, wherein the P type polysilicon gate electrode is disposed adjacent to the N type polysilicon gate electrode.

18. (new) The dry etching method according to claim 15, wherein the at least one etching stage is conducted using a mixed gas of HBr and O_2.

19. (new) The dry etching method according to claim 15, wherein the at least one etching stage is conducted using a mixed gas of HBr, O_2, and He.